Sy429PrPMC-R32E. Enhanced 32Rx Card

Summary features

- Freescale MPC8548E PowerQUICC III processor with:
  - Embedded PowerPC e5500v2 core at 1.0 GHz
  - 32Kbytes Instruction/data caches
  - 512Kbytes L2 Cache
  - Double Precision FPU
  - Integrated MMU
  - Two Gigabit Ethernet ports
  - Two UART ports
  - I²C Controller
  - External Clock and Sync Inputs
  - 2GBytes DDR2-667 SDRAM
  - Two selectable pages each of 32MBytes NOR Flash
  - PCI Carrier available for peripheral I/O support
  - Intelligent VME Carrier Card with two PMC Sites
  - PIM and Transition Module for VME peripheral I/O support

- Arinc-429 Support providing:
  - Up to 32 channels of Arinc-429 (32Rx)
  - Software selectable ARINC-429 or 575.
  - Backwards compatible with Sycos non-processor PMC cards
  - Interface compatible with 32bit PCI Local bus Specification, Rev. 2.2
  - PMC modules configurable from 4 to 32 channels.
  - Each channel is supported by a 1k deep 4byte wide Cyclic-Data-Buffer. Deeper buffers can be supplied as an option.
  - User Selectable Receiver Current Value Table.
  - Direct access to Cyclic Data Buffer Read / Write Pointers.
  - PCI interrupts on Module Events.
  - Direct access to Module Registers and Application Memory.
  - High Resolution Time-Stamp of each received label.
  - ARINC Input/Output via 68pin SCSI on the front panel.
  - VxWorks, Linux, Windows XX drivers and software tools.
  - Firmware options supporting:
    - ARINC-571, 573 and 582
  - Other modules for supporting:
    - ARINC-561, 568, 571, 582 (6-wire)

Enhanced Receiver Features:

- External Clock and Sync. inputs
- Time-Stamp Resolution selectable from 1μS to 256μS
- Receive Word Count Registers
- Channel Speed selectable from 4kbits/s to 167kbits/s
- Automatic Channel Speed Detection & Selection
- Received Data Error Decoding & Reporting
- Option for channel configuration as Tx or Rx

General Description:
Syco's new range of ARINC 429 PMC modules offer on-board Freescale PowerQUICC III MPC8548E PowerPC processor system support, providing a completely autonomous Arinc-429 communication system. The user has up to 32 Arinc-429 channels on a single width PMC module. Each channel can be programmed independently to operate at a variety of speeds from 4kbits/s to 125kbits/s.

Two user-selectable pages of NOR Flash, each 32Mbytes, provide the user with a powerful environment for developing application software under Linux with VxWorks driver support. Applications can be developed and downloaded to the second page of NOR Flash to make this product fully autonomous from power-up.

The design provides for a wide variety of Arinc-429 channel mix, from a minimum of 4Tx or 4Rx through to 32Tx or 32Rx. Each receive channel is supported by a high resolution time-stamp of received data. Options for channels configurable as Tx or Rx are also available.

Each channel is supported with a Cyclic-Data-Buffer which is 1k deep and 32bits wide. Deeper buffers are available as an option. The receive data time-stamp is stored in a separate cyclic buffer, one for each channel, in parallel with the received data.
Alternatively, the receive data can be stored in the form of a Current Value Table addressed by channel/sdi/label. The time-stamp data is also stored in memory addressed by channel/sdi/label. Cyclic Buffer or CVT is selectable on a per channel basis.

ARINC Input/Output is via a 68 pin SCSI connector on the PMC module faceplate. Provision is made for a Connector Identification Code to be read from the connector.

Sycos PMC modules are 100% backwards compatible with their standard non-processor PMC range of cards, which have been in service since 2004.

Other PowerPC processor PMC modules supporting the six wire buses of ARINC-561, 568, 571 and 582 are available.

The module provides configuration registers which allow the host to:

- Automatically identify the module and its revision status.
- Identify connector cables connected to the module.
- Assign address space for the module’s data buffer memory and registers. (Plug-in and Play).
- Control and monitor the PCI bus interface to the module.
- Read module interrupt configuration as assigned by the POST software as it initialises and configures the system.

Additional features designed into the module are:

- Independent Cyclic-Data-Buffer per channel, each with a capacity for 1k x 4 byte words. Deeper Cyclic-Data-Buffers can be provided as an option.
- Direct access to the Cyclic-Data-Buffer Read / Write Pointers.
- High resolution time-stamping of received data.
- PCI interrupts on Module Events.
- Direct access to Module registers and application memory.
- Interface compatible with 32bit PCI Local Bus Specification, Revision 2.2.

The PrPMC module is designed to be used in a "Plug-in and Play" environment which is made possible, not only by the choice of PCI interface, but also by the provision of various identification and module present registers. These include:

- Device ID
- Vendor ID
- Subsystem ID
- Subsystem Vendor ID
- Connector ID / Present
- Module ID

Using these registers the host can detect the presence of the module and its connector, determine if this is consistent with system requirements and respond accordingly by configuring the system or reporting system deficiencies.

**Cyclic Data Buffers:**

The PrPMC module provides high speed interfacing to up to 32 Cyclic-Data-Buffers to support transmission and reception of ARINC-429 words. Data communication and control can be from either the on-board PowerPC processor or through the PCI interface to the PMC carrier card.

The user is free to read and write to any of the Cyclic-Data-Buffers independent of their type (Tx or Rx). However, the Cyclic-Data-Buffer data transfer system only responds in strict accordance to the channel type. That is, it will transfer data, written to a Tx Cyclic-Data-Buffer, to the appropriate module channel and write received data to the corresponding Rx Cyclic-Data-Buffer.
The Cyclic-Data-Buffers are controlled according to simple rules. The buffer read and write pointers can be read by the host to assist in the data transfer process.

In practice, the user writes data for transmission to consecutive long word locations in the Cyclic-Data-Buffer. Only valid words are transmitted.

Receive data is automatically written to consecutive locations in the Cyclic-Data-Buffer or, in the case of Current Value Table (CVT) organisation is by channel/sdi/label.

**Interrupt Facilities:**

PCI interrupts can be generated for both DMA and Module events. Interrupt Control and status registers are provided for enabling interrupts and determining which events created an interrupt.

The PMC module has been designed to be compatible with Sycos PCI card range. Consequently, interrupts respond in a hierarchical manner, according to which block of eight channels caused the interrupt. The channel which caused the interrupt can then be determined by reading a status register.

For example, in a PMC module that has 8Tx,8Rx, this is equivalent to two blocks of 4Tx,4Rx (block 0 and block 1). If an interrupt is desired when data is first detected on receive channel 0 of block 1, the PCI Interrupt Control is programmed to generate an interrupt from block 1. A local interrupt status register assigned to block 1 can then be read to determine which channel of block 1 caused the interrupt.

**Module Control:**

Separate user manuals are provided for each PMC module. Modules have a minimum of 8 channels and maximum of 32 channels, which are used for either transmission or reception of data. Modules also have registers and memory accessible to the user. Access to this register and memory address space is relatively slow compared with that of the Cyclic-Data-Buffers and is therefore only intended for configuration and control purposes.

**Transmit and Receive System:**

Data written to a Transmit Cyclic-Data-Buffer is automatically transferred to the corresponding transmitter in a manner which ensures the maximum usage of the ARINC-429 data bus. That is, while data is available, ARINC-429 data is transmitted with the minimum 4-bit gap between data words.

Similarly, received data can be captured at this maximum data rate and is automatically transferred to the corresponding Cyclic-Data-Buffer or CVT from where it can be easily transferred over the PCI interface to either the PowerPC host processor memory or the PC host processor memory. Time-stamping of received data is stored in separate cyclic buffers or CVT.

For modules with blocks of 4Tx,4Rx the individual transmitter outputs can be internally looped-back on to the corresponding receive channel. When a channel is configured in this way its transmit driver outputs are disabled to prevent the test signals being received by other equipment on the ARINC-429 data bus.

PCI interrupts can be triggered immediately following reception of complete ARINC-429 data words. The interrupts are controlled and handled in a hierarchical manner so that the reception of ARINC-429 data generates a module interrupt on the mother card which generates a PCI interrupt to the host computer.
Mechanical Description:

The PrPMC module mechanical design conforms to Common Mezzanine Card Standard P1386 [1].

The design allows for up to 32 channels of ARINC-429 interfacing to be provided on a single width PrPMC module, with Input/Output via a 68 pin SCSI connector on the front of the module and through backplane I/O.

Base modules capable of supporting 16 or 32 channels are available. Each card is configurable in blocks of 4Tx and 4Rx. A PMC card can be supplied with at minimum 4Tx or 4Rx. Maximum configurations of (16Tx,16Rx) or 32Tx or 32Rx can be supplied.

A Conduction Cooled version is now available, whose specification is based upon VITA 20-199x/D1.9. This product will support up to 32 channels of ARINC-429, configurable in blocks of 4Tx or 4Rx.

Enhanced Version. Sy429PrPMC-RT32E

Enhancements include:

- External Clock and Sync. inputs
- Time-Stamp Resolution selectable from 1μS to 256μS
- Receive Word Count Registers
- Channel Speed selectable from 4kbits/s to 167kbits/s
- Automatic Channel Speed Detection & Selection
- Received Data Error Decoding & Reporting
- Synchronized Transmissions
- Hardware Transmit Scheduler
- Programmable Transmit Errors
- Option for channel configuration as Tx or Rx

External Clock and Sync inputs, both RS422 and TTL compatible, are provided to enable synchronized transmission and time-stamping of received data. This also enables multiple PMC cards to use the same clock and sync signals.

Received data is automatically time-stamped with a 32-bit clock that has software selectable resolution from 1μS to 256μS. The choice of Cyclic Buffer and Current Value Table organization for the receive data buffers is on a per channel basis. The user can decide to set some channels up as cyclic buffers and others as CVT buffers, as the requirement dictates.

Each transmitter can be enabled or disabled by writing a single word to the Transmit Enable/Disable register. This provides the ability to synchronize all transmitters to within 1/2 bit time. Transmit Cyclic Buffers can be loaded prior to being enabled.

Each transmitter has its own cyclic data buffer, where data for transmission is loaded. A facility has been added to enable transmissions to be timed out onto the bus, thereby giving the user a transmit scheduling facility. A separate parallel cyclic buffer is provided for each transmit buffer, where words are written that determine the gap between transmissions. Each bit of the 16-bit word written adds a 1-bit gap between transmissions. So, a word value of four puts a standard 4-bit gap between transmissions. A word value of 8 puts an 8-bit gap before the next word is transmitted etc.

At 100kbits/s a word gap value of 2^16 (65536 bits) gives 655,360mS gap between words.

The user is also provided with a choice of applying the gap word after the data word or before the data word, thereby enabling delays before words are transmitted.
Errors can be programmed into the transmissions. These errors include:

- 4-bit or n-bit gap between transmissions
- 31, 32 or 33 bit data words.
- Odd Parity, Even Parity or No Parity generation
- Channel Speed selectable from 4kbits/s to 167kbits/s

Error detection is reported for the following:

- gap error
- word length error
- Odd Parity, Even Parity or No Parity Checking

Each receiver is supported with its own word counter. When read, the counter is reset, so that the word count between reads is known.

Channel speed detection logic provides automatic Rx speed setting to High or Low speed. This logic is continuously active and a status register can be read to examine each Rx channel speed.

ARINC Input/Output is from the front panel connector. Clock and Sync inputs are from the PMC I/O connector.

A block diagram of the overall system is provided below.

Two Gigabit Ethernet ports and two UARTs are routed to the PMC rear I/O connector. An external clock and sync input is also routed to the PMC rear I/O as differential RS422.

Functional Block Diagram of the Sy429PrPMC-RT32E.
A functional block diagram of the Arinc-429 sub-system with one RT44 Sub-module configured is shown in the figure below.

Functional Block Diagram of the Arinc-429 sub-system.
## Ordering Information and Variants:

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<th>Forced Air Cooled</th>
<th>Description</th>
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<tbody>
<tr>
<td>Sy429PrPMC-RT32</td>
<td>PrPMC base card, configurable up to 16Tx, 16Rx ARINC-429 channels</td>
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<tr>
<td>Sy429PrPMC-T32</td>
<td>PrPMC base card, configurable up to 32Tx ARINC-429 channels</td>
</tr>
<tr>
<td>Sy429PrPMC-R32</td>
<td>PrPMC base card, configurable up to 32Rx ARINC-429 channels</td>
</tr>
<tr>
<td>Sy429PrPMC-RT88</td>
<td>PrPMC base card, configurable up to 8Tx, 8Rx ARINC-429 channels</td>
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<tr>
<td>Sy429PrPMC-T16</td>
<td>PrPMC base card, configurable up to 16Tx ARINC-429 channels</td>
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<tr>
<td>Sy429PrPMC-R16</td>
<td>PrPMC base card, configurable up to 16Rx ARINC-429 channels</td>
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<tr>
<td>Sy429PrPMC-C16</td>
<td>PrPMC base card, 16 channels configurable as Rx or Tx</td>
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